Claim Rejections – 35 USC § 103

15. Claims 1-27 are rejected under 35 U.S.C. 103(a) as being unpatentable over Wojnaowski et al in view of Howard et al.

16. The inventor respectfully draws a different conclusion when examining Wojnarowski 5,525,190 versus the invention currently under examination. In the drawings and explanations by Wojnarowski the potential for a Z axis electrical connection is shown as in Fig. 12 elements 160, 162',162. However, Wojnarowski does not demonstrate the use of this connection as the conduit for carrying the signal content that the current application clearly shows. In the current application the pad and via hole that connect to the surface device are the same that connect to the optical generation element. In Wojnarowski the connections may be for DC power as well as other uses. Additionally referring to Fig. 14 element 154 forms a Z axis connection between electro-optical elements as described. This is opposite the principle used in the current application which states "An optical printed circuit board with electrical connections in the Z axis and optical connections in the X and Y axis according to the present invention..." which is intended to remedy the problem of using optical connections in the Z axis within a printed circuit board. The printed circuit board has several material instabilities that make an optical connection in the Z axis problematic. Additionally, while the Wojnaowski includes the electrical connections no indications are made in the drawings to a Z axis electrical connection between the electro-optical elements and devices on the surface or Z axis electrical connections with each other.

17. Wojnarowski does not contemplate the use of a capacitive layer to support the optical elements.

18. & 19. Howard 5,155,655 does not contemplate the use of directly mounted components on the capacitive layer. In Col. 5 line 1-9 Howard states " an object of the present invention to provide a capacitive printed circuit board (PCB) with a capacitor laminate included within the multiple layers of the laminated board, a large number of devices such as integrated circuits being mounted or formed on the board and operatively coupled with the capacitor laminate (or multiple capacitor laminates) to provide a capacitive function employing borrowed or shared capacitance as described above. In the current application the need for capacitance is not limited to borrowed or shared capacitance as described in Howard and is dictated by the current required by the device within the time domain allowed by the time of cycle operation. Additional advantages are gained in the current application from mounting the optical devices directly on the layer " Additionally the preferred embodiment views the mounting of these devices on the conductive layer, most preferably copper as a good method of removing heat from the devices due to the large amount of a very good heat conductive material in the copper plane." This heat removal function is considered very important in proper device operation when that device is buried within a printed circuit board.

20. Please review this objection in light of the answers contained in 16-20.

21. Please review this objection in the light of the answer to 16.

22. Separate claims regarding the use of polymer conductive vias have been removed and the claims of 5,6, and 7 have been modified to be non specific to type of material used in the via formation.

23. Please review in the light of the corrected claims.

24,25,26,27. Wojnaroski describes a method of construction that utilizes the formation of a cavity in a PCB structure Fig. 12 which is followed by a dielectric coating in Fig 13 to permit the addition of a second level of electro-optical device built adjacent to the same dielectric layer that the original cavity was in direct interface with. The methods described in Wojnarowski do not readily permit the placement of devices on any internal layer within, as an example, a 24 layer PCB. The current application under consideration provides a scheme by which any internal plane layer may host the optical devices without difficulty. It is this ease of placement that is considered to be a significant advantage over the current art.

28,29,30,31,32,33. Please refer to the corrected claims.

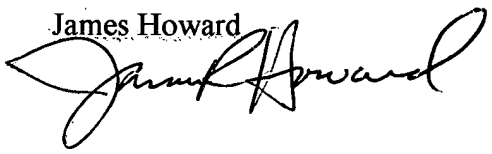
Attachments:

1) Corrected claims (2 pages)
2) Corrected informal drawings (3 pages)
3) Corrections in text (pages 5,6,7,8) to reflect new numbering requested by examiner for drawing figures.

I respectfully submit the above information for your review.

Best Regards,

James Howard



New Claims Without Markings

What is claimed is:

1. A printed circuit board (PCB), comprising:

   multiple layers laminated about optical generation, transmission and reception elements formed on a capacitor laminate,

   the capacitor laminate including;

   two sheets of conductive material and one sheet of intermediate dielectric material,

   the optical elements including;

   a generation device,

   a transmission element to provide an optically clear path between generation and reception elements,

   and a reception device;

   wherein at least one of the optical elements is electrically connected in the Z-axis to at least one printed circuit board element or surface device.

2. The PCB of claim 1 wherein the optical transmission paths are formed by selectively removing areas of the conductive material of the capacitor laminate and placing an optically conductive fiber connecting the optical generation device and the optical reception device.

3. The PCB of claim 1 wherein the optical transmission paths are formed by selectively removing areas of the conductive material from the surface of the capacitor laminate and placing an optically conductive polymer path connecting the optical generation device and the optical reception device.

4. The PCB of claim 1 wherein the optical transmission paths are formed by selectively removing areas of the conductive material from the surface of the capacitor laminate and a clear or open channel is formed within the PCB.

5. The PCB of claim 2 wherein the optical generation device and the optical reception device are connected though the Z axis to other PCB elements by the use of blind, buried or subcomposite vias.

6. The PCB of claim 3 wherein the optical generation device and the optical reception device are connected though the Z axis to other PCB elements by the use of blind, buried or subcomposite vias.

7. The PCB of claim 4 wherein the optical generation device and the optical reception device are connected though the Z axis to other PCB elements by the use of blind, buried or subcomposite vias.

8. The PCB of claim 5 in which multiple layers of optical elements formed on capacitor layers are laminated within the PCB.

9. The PCB of claim 6 in which multiple layers of optical elements formed on capacitor layers are laminated within the PCB.

10. The PCB of claim 7 in which multiple layers of optical elements formed on capacitor layers are laminated within the PCB.

11. A printed circuit board (PCB), comprising:

multiple layers laminated about optical generation, transmission and reception elements the optical elements including;

a generation device,

a transmission element to provide an optically clear path between generation and reception elements,

and a reception device;

wherein at least one of the optical elements is electrically connected in the Z-axis to at least one printed circuit board element or surface device.

12. The PCB of claim 11 wherein the optical generation device and the optical reception device are connected though the Z axis to other PCB elements by the use of blind, buried or subcomposite vias.